Signal and Power Integrity Seminar/Workshop

Education Duration :1 Day

Education Language : English - Italian

Tranier : Pietro Vergine

Prerequsite : -

Target Audionce : -

Content :

The objective of this workshop 1 day is to understand the root causes of Signal Integrity issues from a theory point of view and see how those can be analyzed using EDA tools available on the market.

Several examples will be demonstrated to fix the concepts learned.

During the workshop we will also look at the methodologies' aspects to properly address the design of a robust and reliable PCB in terms of Signal and Power Integrity looking at some of the tools available today on the market (mainly based on Mentor Graphics tools but not only).

Agenda :

Signal Integrity and EMC: the root cause
Models and tools for simulation
Inductance, Transmission Lines and Reflections
Crosstalk
Differential Signal
Losses
Power Integrity
Emissions
Design partitioning, Stackup
Modeling Discontinuities
Mention to Measurements Instruments

There is no prerequisite required to attend this workshop in terms of tool usage as the presenter will run the examples.

HyperLynx Signal Integrity Analysis

Education Duration : 3 Days

Education Language : English - Italian

Tranier : Pietro Vergine

Prerequsite : -

Target Audionce : Design and Verification Engineers

Content :

The HyperLynx Signal Integrity Analysis 3 days course will help you understand basic signal integrity, crosstalk, EMI concepts, and pre- and post- layout stages of the design process.

Hands-on lab exercises will reinforce what is discussed during the lectures and provide you with extensive tool usage experience under the guidance of our industry expert instructors.

You Will Learn How To

- Create and simulate LineSim free-form schematics
- Investigate termination strategies
- Investigate stack-up strategies
- Translate design databases
- Identify and debug SI and Crosstalk issues
- Simulate EMC and evaluate the results
- Assign models and component values
- Evaluate SI and Crosstalk issues
- Translate PCB layout databases
- Run BoardSim simulations interactively and in batch mode
- Run BoardSim for both single and multi-board projects
- Evaluate batch mode simulation reports to identify potential problems
- Run Sweep analysis and explore a solution space

Hands-on Labs

Throughout this course, extensive hands-on lab exercises provide you with practical experience using HyperLynx SI software. Hands-on lab topics include:

- LineSim free-form schematic creation, editing stack-up, assignment of models and component values

- Compare theoretical values with simulation results
- Manual and automatic waveform measurements of overshoot, flight-time and crosstalk
- Evaluating the effects of different impedance matching strategies, topologies, technologies, and stack-ups in LineSim Sweeping design parameters
- Create and debug IBIS models
- Add model libraries using different methods in BoardSim
- Perform Batch Mode Quick Analysis in BoardSim and review the report
- Perform Batch Mode Detailed Analyses in BoardSim and analyze the reports
- Interactively simulate different scenarios to fix problems in BoardSim
- Document changes made in BoardSim Set up and simulate nets between boards using multi-board projects

HyperLynx Power Integrity Analysis

Education Duration: 2 Days

Education Language : English - Italian

Tranier : Nigel Woolaway

Prerequsite : Familiarity with High Frequency design concept, familiarity with Windows platform, Familiarity with Hyperlynx user interface

Target Audionce : -

Content :

In this 2 days course you will learn how to

- Create and simulate a Power Distribution Network (PDN) in LineSim®
- Set up and run DC Drop Power Analysis in LineSim and BoardSim®
- Set up and run Decoupling Analysis in LineSim and BoardSim
- Set up and run Plane Noise Analysis in LineSim and BoardSim
- Set up and run Power Integrity/Signal Integrity co-simulation in LineSim
- Extract Via and PDN models for use in various simulation environments
- Analyze bypassing of signal vias
- Evaluate the results of different types of analysis and identify the potential hot spots in PowerScope, TouchStone Viewer, and Digital Oscilloscope graphical tools
- Modify the PDN to fix the potential problems
- Explore design PDN methodologies

Hands-on Labs

- Using the LineSim PDN editor to create board outlines and shapes, add pins for representing power sources/sinks on a PCB, and assign models to the pins for what-if pre-layout DC Drop analysis
- Performing DC Drop analysis in LineSim, evaluating the analysis results, identifying the potential problems, making appropriate modifications, and validating the modifications through re-simulating
- Assigning models to the board's IC power supply pins in BoardSim and simulating the design for interactive and batch post-layout DC Drop analysis
- Using PowerScope graphical tool to view DC voltage drop plots, current density/distribution on the board's various power planes
- Using the LineSim PDN editor and decoupling analysis wizard to explore how decoupling capacitors and board stackup affect the impedance of a power distribution network in pre- and post-layout simulations
- Evaluating the impedance profile of a PDN in the TouchStone Viewer
- Analyzing how AC changes in IC power pins affect the noise on power planes, exploring the analysis results in PowerScope, identifying the hot spots, making adjustments (changing board shape, etc.) in LineSim, and re-simulating to validate the adjustments
- Setting up and performing signal Integrity / power integrity co-simulation, evaluating signal integrity simulation results in the digital oscilloscope graphical tool and power integrity results in PowerScope
- Analyzing the bypassing quality of a signal via
- Exploring various methodologies for designing a PDN

HyperLynx DDRx Interface Analysis

Education Duration : 2 Days

Education Language : English - Italian

Tranier : Pietro Vergine

Prerequsite : Familiarity with High Frequency design concept, Hyperlynx interface and Windows OS

Target Audionce : Hardware Designers and Digital Signal Processing Specialists

Content :

The HyperLynx DDRx Interface Analysis 2 days course will help you gain an in-depth understanding of DDRx interfaces and how to use the HyperLynx software to analyze signal integrity, crosstalk, and timing of DDRx in both pre- and post- layout stages of the design process.

Hands-on lab exercises will reinforce what is discussed during the lectures and provide you with extensive tool usage experience under the guidance of our industry expert instructors.

You will learn how to

- Identify different DDRx interface types
- Calculate the data rate and frequency for DDRx address and data busses
- Set up the DDRx Wizard in LineSim and BoardSim
- Interpret the timing parameters at the DRAM and DDRx controller by using the DDRx Wizard
- Create timing models for a DDRX controller
- Interpret the DDRx analysis results Perform timing analysis for the DDRx interface
- Calculate the jitter margins
- Use the write leveling options in DDrx Wizard

Hands-on Labs

Throughout this course, extensive hands-on lab exercises provide you with practical experience using HyperLynx SI software. Hands-on lab topics include:

- Preparing the DDRx Wizard for pre- and post-layout analyses
- Preparing IBIS buffer models for DDRx analysis
- Deriving timing parameters for a controller timing model Creating timing model for the controller
- Setting up the DDRx Wizard
- Running and analyzing the result of timing simulation
- Simulation and analyzing jitter results
- Simulating and analyzing round-trip time results for DDRx interface
- Simulating and analyzing write leveling options

HyperLynx High-speed Serial Interface Analysis

Education Duration : 2 Days

Education Language : English - Italian

Tranier : Pietro Vergine

Prerequsite : Familiarity with high frequency design concept and Hyperlynx interface

Target Audionce : Hardware Designers and Digital Signal Processing Specialists

Content :

The HyperLynx High-Speed Serial Interface Analysis 2 days course will help you gain an in-depth understanding of high speed serial interfaces e.g. SERDES and how to use the HyperLynx software to analyze their signal integrity, crosstalk, and timing in both pre- and post- layout stages of the design process.

Hands-on lab exercises will reinforce what is discussed during the lectures and provide you with extensive tool usage experience under the guidance of our industry expert instructors.

You will learn how to

- Identify high-speed serial interfaces
- Distinguish between parallel and serial interfaces
- Explore factors affecting a high-speed channel performance in LineSim
- Make trade-offs from simulation results
- Generate physical constraints for the serial interface
- Create post-layout SERDES channel topology
- Assign models to various component on a SERDES channel
- Simulate an eye diagram using the Fast Eye Wizard
- Use IBIS-AMI channel analyzer to simulate SERDES channels
- Implement a 3D via model and simulate it in LineSim

Hands-on Labs

Throughout this course, extensive hands-on lab exercises provide you with practical experience using HyperLynx SI software. Hands-on lab topics include:

- Exploring the a PCI Express SERDES design
- Planning stackup for pre-layout analysis of a SERDES channel
- Analyzing loss for various configurations of the channel

- Checking for the transmitter and receiver compliance
- Simulating to derive constraint for the entire SERDES channel
- Verifying a SERDES channel in post-layout mode
- Setting up advanced connector models for MultiBoard projects
- Simulating with the FastEye Wizard
- Using IBIS_AMI channel analyzer wizard
- Creating and simulating 3D via models

HyperLynx DRC

Education Duration : 2 Days

Education Language : English - Italian

Tranier : Pietro Vergine

Prerequsite : Familiarity with High Frequency design concept, Hyperlynx SI and PI products and Windows operating system

Target Audionce :

Content :

HyperLynx DRC 2 days course will help you gain the ability to use HyperLynx DRC environment to check for violation of standard built-in design rules in your PCB. You will learn how to configure the rules, how to run them and how to evaluate the results and cross probe any rule violation back into your PCB. Hands-on lab exercises will reinforce lecture and discussion topics under the guidance of our industry expert instructors. This course is offered on Windows platform.

You will learn how to

- Navigate in and use the GUI of HyperLynx DRC software
- Set up your DRC projects and assign models
- Import designs into HL DRC environment
- Define object lists
- Use standard SI, PI, and EMI rules
- Run checks
- Examine the results

Hands-on Labs

- Exploring all areas and functions of the user interface

- Opening a design
- Creating object lists
- Assigning models
- Associating rules with object lists
- Running checks
- Examining violations

Signal Integrity and High-Speed Methodology

Education Duration : 3 Days

Education Language : English - Italian

Tranier : Pietro Vergine

Prerequsite : -

Target Audionce :

Content :

This 3 days lecture modules address transmission lines and their effects on digital circuitry and printed circuit boards. Our industry expert instructors will lead you through detailed examples from real-world designs to demonstrate the necessity of understanding signal integrity issues and applying sound signal integrity principles to your designs. Specific tools are rarely discussed and therefore the class is appropriate for all Engineers involved in high speed digital pcb designs.

You will learn how to

- Transmission lines and their effect on digital circuitry
- Printed circuit boards: Zo, Zdiff, stackup, plane placement, crosstalk
- Termination, topology, timing, parasitics, etc
- Differential pair: routing, timing, crosstalk, common mode, terminating, multi-GHz
- Crosstalk: microstrip vs stripline, forward & reverse, timing & jitter, understanding and preventing
- Power integrity: planes, capacitors – ESL, size, location, mounting inductance
- Reference planes: ground, power, return currents, splits, crosstalk, stitch caps
- Vias: reference changes, stub lengths, stackup, impedance
- Connectors: pinouts for high speed return current & crosstalk
- High Speed Layout: vias, connectors, capacitors, PCB losses, planes

- S Parameters
- Testing Issues: equipment, probes, test points
- Models: IBIS, drivers, receivers, simulators and accuracy

Key topics:

What is a transmission line?

- What causes transmission lines
- What do they do to digital circuitry
- Avoiding transmission line problems

Transmission Line Effects

- Undershoot & Overshoot – can destroy boards
- Ringback, monotonicity, crosstalk , timing

Printed Circuit Boards

- Stackup
- Making controlled Zo
- Controlled Zo or controlled distance
- Crosstalk problems with multiple vendors

Drivers, Receivers, Zo

- Strength & speed
- Zo & drivers
- Incident vs. reflected wave switching

Board Interconnect Delay

- How it is different than system delay
- Need to include interconnect delay in timing
- How it is calculated
- Receiver input C, driver output Rs, PCB Zo, etc
- Reflected vs. incident wave switching

Termination

- When it is necessary
- Required to stop undershoot and overshoot
- Placement and stub length
- Parallel, series, Zo matching, driver Rs matching
- Diodes – dangerous

Topologies

- When are topologies important
- How do topologies affect signal integrity & timing
- Short & long Tee, star, daisy chain
- Stub length

Package Parasitic

- L's, C's and R's
- How do they affect signal integrity & timing
- Capacitive loading on transmission lines

Differential Pair

- Why are they important
- Noise and EMI
- Layout issues
- Zdiff, Zcomm, Zeven, & Zodd
- Controlling Zdiff
- Side to side vs broadside (over/under)
- Weak vs strong coupling
- Zdiff problems
- Skew affects on signal integrity & timing
- Better terminations
- How to make differential pair for > 3 GHz

Crosstalk

- What causes crosstalk
- Routing densities
- Effects on timing & signal integrity
- Microstrip vs stripline are different
- Same layer vs dual stripline over/under
- Differential pair crosstalk
- Fixing crosstalk
- What needs to be done by layout engineers

Groundbounce – SSN

- What causes groundbounce
- What does it do to driver & receiver voltage levels
- Problems with FPGA's and ASIC's

PCB Power Integrity

- Planes
    - Power & ground
    - Spacing & location – loop inductance
- Bypass Capacitors
    - ESL
    - Package & size uf
    - Spacing to load
    - Location on PCB & empty spaces
    - Mounting inductance, via placement, spacing, pads etc

Reference Planes

- Perforation
- Crossing splits
- Reference consistency in designs
- Vias, layer changes & references
- Controls routing & stackup Connectors

- Controlled Zo, geometry, pinouts
- Reference consistency
- Coupling
- How many grounds & Vccs – return currents

Vias

- Zo changes
- Reference changes
- Stub lengths
- Blind & buried vias
- Pads, antipads, hold diameter
- How to make a 10 GHz via

AC Losses

- Skin effect & dielectric loss
- Microstrip vs stripline
- Noise margins with differential pair
- Pre-emphasis & equalization

Layout Issues

- Boards are becoming more difficult to layout
- What issues are important in today's fast boards for layout
- PCB's are now part of the design

Testing Issues

- Faster boards are harder to test
- How do you test them
- What equipment do you need
- How fast does the equipment need to be

S Parameters

- Frequency dependent descriptors

- Good for gigahertz designs
- S21 – Insertion loss or interconnect loss for SI
- Includes discontinuities, connectors, packages
- VNA – 2 & 4 port networks

IBIS Models

- Drivers & receivers
- Simulators
- Accuracy
- Repairing and modifying

Quality Board Designs

- How to make quality boards
- What tools are needed
- Signal integrity issues must be included

Signal and Power Integrity Essentials Training

Education Duration : 5 Days

Education Language : English -Arabic

Tranier : Dr. Alaa Elrouby

Prerequsite : -

Target Audionce :

Content :

Signal Integrity is defined as the branch of science that concerns with the design, analysis and validation of the signals' quality and timing when transmitted from the driver to the receiver over the interconnect. This training is designed to cover the essentials of the five main components of signal integrity analysis (namely: transmitter, receiver, signal quality, timing and interconnect) as well as the power integrity and its interactions with signal integrity.

The training is a combination of theoretical and lab (simulation) sessions for a total of 40 hours. The lab sessions are based on HyperLynx SI/PI simulation tool.

The details of the training modules

Signal integrity Overview
Importance of SI/PI in modern digital system – definition of main parameters for signal timing and signal quality – industrial trends and modern SI/PI challenges – SI related measurement equipment – digital system design cycle.

Non-ideal Transmission Lines
Metallic and dielectric losses – surface roughness – frequency dependence effects – serpentine and bend effects – inter-symbol-interference (ISI).

Transmission Line Lab.
PCB stackup – simple net simulation – different termination schemes – under and over driven nets – lossy TL – surface roughness – inter-symbol-interference

Crosstalk
Crosstalk types and their behaviors – mutual impedance – even and odd modes and their characteristics – termination techniques – crosstalk minimization

Crosstalk Lab.
Crosstalk analysis – vertical and lateral crosstalk – number of neighbors to consider- grounded trace for shielding – even and odd mode crosstalk

VIA's, Packages and Connectors
VIA model and impact on SI – package types and modeling – connector types, models and impact on SI – induced crosstalk noise in connectors and packages – noise reductions rules

Non-ideal Return Paths
Current return path and its impact on SI – return path discontinuity – dependency on buffer type – solutions for return currents discontinuity – simultaneously switching noise (SSN)

Digital Timing Analysis
Common-clock timing calculations and limitation – source synchronous system timing limitations and modifications – setup and hold margin calculations for different systems

DDR2 Lab.
Single ended nets – differential DQS net – net length effect on timing and signal quality – single-ended and differential crosstalk analysis – DDR2 timing analysis

Differential Signaling
differential signals definition and characteristics – advantages and disadvantages – even/odd mode and their relation to diff/comm modes – design rules – coupling factor – termination techniques – differential losses – multi-mode scattering matrix

Serial Communication
Serial communication parameters and definitions – inter-symbol-interference (ISI) – block coding – eye diagram – equalization and pre-emphasis – Serial communication link.

USB and SERDES Channel Analysis Lab.
USB tutorial – eye diagram simulation – TL losses – simple channel analysis – PCI express with capacitive coupling

Power Delivery System (PDS)
PDS definition, functionality and building blocks – power planes – power supply types and models – power delivery dynamics – capacitors modeling, mounting and characteristics – PDS design methodology – decoupling solutions

Power Integrity Lab.
Pre-/post- layout DC drop analysis – single net analysis – batch analysis – decoupling analysis – stackup effect – plan noise analysis – reference plane discontinuity – capacitor mounting and position and their effects- SI/PI co-simulation